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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,554	IIDA, IZUO	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-21* is/are pending in the application.

4a) Of the above claim(s) *4-10,17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,11-16 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant filed a response on 3/8/04 to the non-final Office Action mailed 2/24/04. Applicant's response notes that the 2/24/04 Office Action did not consider the amendment filed 2/3/04. The rejections in the 2/24/04 Office Action are vacated as they did not treat the claims as they were pending at that time, i.e. including the amendment of 2/3/04. This Office Action is in response to applicant's response filed 3/8/04 and considers the claims as amended in the 2/3/04 amendment.

2. In applicants amendment filed 9/23/03 and reiterated in the amendment filed 2/3/04, claim 16 has been amended in response to the rejection under 35 U.S.C. 112, first paragraph. Upon further review of the application, the examiner has determined that the previous 35 U.S.C. 112, first paragraph rejection was improper as the specification did enable the "selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS transistor is to be formed." See specification page 11 lines 11-14. Thus, the examiner acknowledges that claim 16 as originally presented met the requirements of 35 U.S.C. 112, first paragraph. However, claim 16 as currently amended does raise issues of new matter and will be treated accordingly below. For the sake of art rejections, the examiner will consider claim 16 as originally presented and supported by the specification such that a proper determination of it's patentability over the prior art can be achieved.

Claim Objections

3. Claims 19-21 are objected to because of the following informalities: These claims recite a dimension (approximately 150 nanometers) but do not state what that dimension represents. In light of the arguments presented and the specification the dimension seems to be referring to the thickness of the gate insulating film. It is suggested that these claims be amended to recite "approximately 150 nanometers thick." Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 16 as currently amended is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 16 as currently amended recites the limitation "selectively etching the tunnel insulating film **except from** on the region of the semiconductor substrate where the MOS transistor is to be formed." This limitation was not described in the specification as originally filed. As can be seen in figure 6, the tunnel insulator 16 is not etched in the region of the memory cell but instead remains between the floating gate 14 and the control gate 17. Though not

explicitly labeled, it appears that the tunnel insulator 16 remains on most portions of the substrate.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1, 3, 11-16 and 19-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. The term "high voltage" in claims 1, 11 and 13 is a relative term which renders the claim indefinite. The term "high voltage" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. One of ordinary skill in the art would not know what voltage needs to be applied to the transistor to render the transistor a “high voltage” transistor.

9. The term "thick" in claims 1, 11 and 13 is a relative term which renders the claim indefinite. The term "thick" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. One of ordinary skill in the art would not know what thickness the oxide would need to be formed to in order to be considered a “thick” oxide.

10. Insofar as definite, the claims are rejected over the prior art as follows.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 3, 11-15 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komori et al. (U.S. Patent No. 5,656,522) in view of Hsieh et al. (U.S. Patent No. 6,165,845).

Komori et al. teaches in figure 4 and on column 5 lines 34-36 and column 8 lines 23-33, a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, the method comprising simultaneously forming the oxide film 8 on the floating gate 7a of the non-volatile memory cell transistor and a gate insulating film 8 of the MOS transistor in a single thermal oxidation step. Komori et al. does not teach selectively forming the oxide film on the floating gate. Komori et al. also does not explicitly disclose the MOS transistor being a "high voltage" MOS transistor or the gate insulating film of the MOS transistor being a "thick" gate insulating film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach selectively forming the oxide on the floating gate in figure 3f. The oxide formed by Hsieh et al. is a "thick" oxide as it is formed to a thickness of 1000 to 1800 angstroms (col. 7 lines 7-8).

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to selectively form the oxide film on the floating gate using the oxidation process taught by Hsieh et al. In combining the oxidation process taught by Hsieh et al. with the simultaneous formation of the oxide film on the floating gate and gate insulating film of the MOS transistor as taught by Komori et al. the gate insulating film would be formed "thick." With the gate insulating layer formed "thick" the MOS transistor is considered a "high voltage" MOS transistor as it would be able to withstand a "high voltage" during operation without breaking down. The motivation for combining the references is to provide a gate bird's beak to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 1.

With regard to claim 11, Komori et al. teach a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate. Specifically, Komori et al. teach forming a silicon layer 7a on the substrate 1 (figure 3, column 8 lines 9-21), selectively removing the silicon layer on

a region of the substrate where the MOS transistor is to be formed (figure 3, column 8 lines 9-21), and simultaneously forming an oxide film 8 on the region where the floating gate is to be formed and a gate insulating film 8 on the region where the MOS transistor is to be formed (figure 4). Komori et al. do not teach forming an oxidation-resistant film over a first entire resulting surface, selectively removing the oxidation resistant film on the region of the substrate where the MOS transistor is to be formed and on a region of the substrate where the floating gate of the non-volatile memory cell transistor is to be formed, selectively forming the oxide film on the region where the floating gate is to be formed, or forming a tunneling insulating film over the gate insulating film. Komori et al. also does not explicitly disclose the MOS transistor being a "high voltage" MOS transistor or the gate insulating film of the MOS transistor being a "thick" gate insulating film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach forming an oxidation resistant film 50 over a first entire surface (figure 2b) and selectively removing the oxidation-resistant layer on the region where the floating gate of the non-volatile memory cell transistor is to be formed (figure 2c). Hsieh et al. then teach selectively forming an oxide film 45 on the region where the floating gate is to be formed (figure 2d) and forming a tunneling insulating film 50 over the gate insulating film 45 (figure 2f). The oxide formed by Hsieh et al. is a "thick" oxide as it is formed to a thickness of 1000 to 1800 angstroms (col. 7 lines 7-8). In combining the two references, it would be obvious to one of ordinary skill in the art a the time of the invention that the oxidation resistant film would be selectively removed on the region

where the gate insulating film of the MOS transistor is to be formed as the process of Komori et al. teach forming the oxide on the floating gate and the gate insulating film of the MOS transistor in the same oxidation step.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an oxidation resistant film on the entire surface and selectively remove the oxidation-resistant film where the floating gate is to be formed and where the MOS transistor is to be formed, to selectively form the oxide where the floating gate is to be formed, and to form a tunneling insulator over the gate insulating film. In combining the oxidation process taught by Hsieh et al. with the simultaneous formation of the oxide film on the floating gate and gate insulating film of the MOS transistor as taught by Komori et al. the gate insulating film would be formed "thick." With the gate insulating layer formed "thick" the MOS transistor is considered a "high voltage" MOS transistor as it would be able to withstand a "high voltage" during operation without breaking down. The motivation for combining the references is to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to form the tunneling insulator to insulate the control gate from the floating gate. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 11.

With regard to claim 3, the oxidation resistant film of Hsieh et al. is taught as a silicon nitride film.

With regard to claim 12, the oxide film is formed by a single thermal oxidation step as taught by Komori et al.

With regard to claim 13, Komori et al. teach a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate. Specifically, Komori et al. teach forming a gate insulating film 6 on the semiconductor substrate 1 (figure 2), forming a silicon layer 7a on the first gate insulating film 6 (figure 3, column 8 lines 9-21), selectively removing the silicon layer on a region of the substrate where the MOS transistor is to be formed (figure 3, column 8 lines 9-21), and simultaneously forming an oxide film 8 on the region where the floating gate is to be formed and a gate insulating film 8 on the region where the MOS transistor is to be formed (figure 4). Komori et al. do not teach forming an oxidation-resistant film over a first entire resulting surface, selectively removing the oxidation resistant film on the region of the substrate where the MOS transistor is to be formed and on a region of the substrate where the floating gate of the non-volatile memory cell transistor is to be formed, selectively forming the oxide film on the region where the floating gate is to be formed, removing at least some of the remaining oxidation-resistant film, or forming a tunneling insulating film over the gate insulating film. Komori et al. also does not explicitly disclose the MOS transistor being a "high voltage" MOS transistor or the gate insulating film of the MOS transistor being a "thick" gate insulating film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach forming an oxidation resistant film 50 over a first entire surface (figure 2b) and selectively removing the oxidation-resistant layer on the region where the floating gate of the non-volatile memory cell transistor is to be formed (figure 2c). Hsieh et al. then teach selectively forming an oxide film 45 on the region where the floating gate is to be formed (figure 2d), removing at least some of the remaining oxidation-resistant film (figure 2e) and forming a tunneling insulating film 50 over the gate insulating film 45 (figure 2f). The oxide formed by Hsieh et al. is a "thick" oxide as it is formed to a thickness of 1000 to 1800 angstroms (col. 7 lines 7-8). In combining the two references, it would be obvious to one of ordinary skill in the art a the time of the invention that the oxidation resistant film would be selectively removed on the region where the gate insulating film of the MOS transistor is to be formed as the process of Komori et al. teach forming the oxide on the floating gate and the gate insulating film of the MOS transistor in the same oxidation step.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an oxidation resistant film on the entire surface, selectively remove the oxidation-resistant film where the floating gate is to be formed and where the MOS transistor is to be formed, selectively form the oxide where the floating gate is to be formed, remove at least some of the remaining oxidation-resistant film, and form a tunneling insulator over the gate insulating film. In combining the oxidation process taught by Hsieh et al. with the simultaneous formation of the oxide

film on the floating gate and gate insulating film of the MOS transistor as taught by Komori et al. the gate insulating film would be formed "thick." With the gate insulating layer formed "thick" the MOS transistor is considered a "high voltage" MOS transistor as it would be able to withstand a "high voltage" during operation without breaking down. The motivation for combining the references is to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to form the tunneling insulator to insulate the control gate from the floating gate. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 13.

With regard to claim 14, the oxidation-resistant film of Hsieh et al. is taught as a silicon nitride film.

With regard to claim 15, the oxide film is formed by a single thermal oxidation step as taught by Komori et al.

With regard to claims 19-21, the selective oxidation step of Hsieh et al. teaches forming the oxide to a thickness of approximately 150 nanometers. In the combination of the two references, the "thick" gate insulating film of the MOS transistor is formed in the same oxidation step and would therefore have a similar thickness. Thus, the references as combined teach the "thick" gate insulating film being approximately 150 nanometers thick.

Response to Arguments

13. Applicant's arguments filed 9/23/03 have been fully considered but they are not persuasive.

Applicant argues that Komori et al. teaches a thin gate insulating film and thus does not teach the "thick" gate insulating film claimed for the "high voltage" MOS transistor. Applicant further states that neither Komori et al. nor Hsieh et al. discloses a "high voltage" MOS transistor requiring the "thick" gate insulator. This argument is not persuasive. As explained in the rejections above, the combination of the two references would result in a "thick" gate insulating film such that the MOS transistor would operate as a "high voltage" MOS transistor. Though not explicitly stated in either reference, it would have been obvious to one of ordinary skill in the art at the time of the invention that when combining the oxidation step of Hsieh et al. into the process of Komori et al. the result would be a "thick" gate insulating film. As far as the record shows, the only difference between a "high voltage" transistor and a "normal voltage" transistor is the thickness of the gate insulating film and thus since the MOS transistor of Komori et al. formed using the oxidation process of Komori et al. has a "thick" gate insulating film it is considered a "high voltage" transistor regardless of whether either reference explicitly states "high voltage" or not.

Applicant also argues that since the gate insulating film of Komori et al. is formed simultaneously as a continuous layer there is no suggestion in Komori et al. that it would be desirable to form the oxide film and the gate insulating film selectively. This is not persuasive as Komori et al. was not relied upon to teach the selective formation of the

films. The selective oxidation was taught by Hsieh et al. as explained in the rejections above.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Last, applicant argues that the Office Action does not identify a location in the references that suggests the desirability of selectively forming the layers in question (i.e. selectively forming the oxide film and the gate insulating layer) and thus no suggestion of the desirability of combining exists. This is not persuasive as motivation for the combination was given in the rejection. Motivation for combining does not have to come from the references themselves. See MPEP 2143.01. Further, the motivation given in the rejection "to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell" can be found on column 1 lines 20-25. Thus, proper motivation has been established and the rejection is considered proper.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571)

272-1736. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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